

# CALL FOR PAPERS

## *IEEE Transactions on Nanotechnology & IEEE Transactions on Emerging Topics in Computing*

### Joint Special Section on VLSI and Nanotechnology Design Trends for Computing Innovations

IEEE Transactions on Nanotechnology and IEEE Transactions on Emerging Topics in Computing seek original manuscripts for a Special Section tentatively scheduled to appear in the September 2017 issues. The topics of interest for this special section include:

- 1. VLSI Design:** Design of ASICs, microprocessors/micro-architectures, embedded processors, digital systems, NoC, interconnects, memories, and FPGAs.
- 2. VLSI Circuits:** digital circuits, chaos/neural/fuzzy-logic circuits, high-speed/low-power circuits.
- 3. Low Power and Power Aware Design:** Circuits, micro-architectural techniques, thermal estimation and optimization, power estimation methodologies, and CAD tools.
- 4. Computer-Aided Design (CAD):** Hardware/software co-design, logic and behavioral synthesis, logic mapping, simulation and formal verification, layout (partitioning, placement, routing, floor planning, compaction), algorithms and complexity.
- 5. Testing, Reliability, Fault-Tolerance:** Digital testing, design for testability and reliability, online testing techniques, static and dynamic defect- and fault-recoverability, and variation-aware design.
- 6. Emerging Technologies & Post-CMOS VLSI:** Analysis, circuits and architectures, modeling, CAD tools and design methodologies for nanotechnologies, molecular electronics, quantum devices, biologically-inspired computing, spintronic technology, CNT, MTJ, NML, PCM, PMC, and sensor and sensor networks, etc.

Submitted articles must not have been previously published or currently submitted for journal publication elsewhere. An extended version of an article appearing in a conference proceedings (and in particular, GLSVLSI 2016) can be submitted provided that it has substantially new content w.r.t. to the original conference version. The conference paper must be cited in the main text and the cover letter must clearly describe the differences with the conference version and clearly identify the new contributions. As an author, you are responsible for understanding and adhering to the submission guidelines. Authors are invited to submit manuscripts focused on topics of computing directly to *Transactions on Emerging Topics in Computing (TETC)* at <https://mc.manuscriptcentral.com/tetc-cs> and papers focused on topics of nanoscale circuits and technology directly to *Transactions on Nanotechnology (TNano)* at <https://mc.manuscriptcentral.com/tnano>. Authors should be aware that papers can be published in TNano or TETC depending on the availability of space with the final allocation at the discretion of the Editor-in-Chief of the respective Transactions. Please address all correspondence regarding this Special Section to the Guest Editors (email: [tpc.chairs@gmail.com](mailto:tpc.chairs@gmail.com)).

#### IMPORTANT DATES:

- Submission deadline: October 31, 2016.
- First decision to authors: February 1, 2017.
- Revisions due: April 1, 2017.
- Acceptance notification: July 1, 2017.
- Publication material due: August 1, 2017.
- Special Section publication: September 2017.

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