CALL FOR PAPERS

IEEE Transactions on Computers & IEEE Transactions on Nanotechnology

Joint Special Section on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

With increasing defect rates in highly scaled CMOS and emergence of alternative nanotechnology devices, defect and fault tolerance in VLSI and nanotechnology systems is of growing importance. The IEEE Transactions on Computers and IEEE Transaction on Nanotechnology seek original manuscripts for a Special Section on Defect and Fault Tolerance in VLSI Systems scheduled to appear in the issue of March 2016. The topics of interest for this special issue include, but are not limited to:

1. **Yield Analysis and Modeling**
   Defect/Fault analysis and models; statistical yield modelling; critical area and metrics.

2. **Testing Techniques**
   Built-in self-test; delay fault modelling and diagnosis; testing for analogue and mixed circuits; signal and clock integrity.

3. **Error Detection, Correction, and Recovery**
   Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; hw/sw techniques.

4. **Dependability Analysis and Validation**
   Fault injection techniques and environments; dependability characterization.

5. **Defect and Fault Tolerance**
   Reliable circuit/system synthesis; radiation hardened/tolerant processes & design

6. **Variability at nanoscale**
   Variation of electrical characteristics of nanoscale devices due to process, aging, temperature etc.

7. **Fault modelling of emerging devices**
   Modeling and analysis of temporary and permanent faults in CNTs, QCA, DNA, RTDs, SETs, molecular devices

8. **Yield and reliability of non-CMOS based memories**
   Defect and fault in PCM RAM, Spin-Transfer-Torque MRAM, memristors based memories etc.

9. **Design tools for DFT**
   New design tools for Defect and Fault Tolerance; applicability of existing algorithms and method to novel technologies; Design of novel tools for next generation nanotechnology systems

10 **Case studies and applications**
   Applications to automotive, railway, avionics, industrial control, biomedicine, space.

The submitted papers must describe original research which is not published nor currently under review by other journals or conferences. Extended conference papers should contain at least 40% new material and will pass through the normal review process. Authors are invited to submit manuscript focused on gate and higher system levels directly to TC (https://mc.manuscriptcentral.com/tc-cs) and papers focused on circuit and lower levels directly to TNANO (https://mc.manuscriptcentral.com/tnano). However, authors should be aware that papers will be published in TC or TNANO depending on the technical content of the paper and the availability of space. The selection will be at the discretion of the Editor-in-Chiefs of the respective Transactions.
With this premise, Authors must clearly indicate their preference for publication in the cover letter. Please address all correspondences regarding this Special Section to the Guest Editors (email: dft_joint_special_section@ing.uniroma2.it). To increase the impact and visibility of their work, Authors of accepted papers will be requested to prepare a short “abstract video” of their manuscript to be published as supplemental material in the TC or TNANO websites.

IMPORTANT DATES
Submission deadline: ~~January 15, 2015~~. February 1, 2015.
First decision to authors: April 15, 2015.
Revision due (if needed): May 15, 2015.
Final notification of acceptance/rejection: July 15, 2015.
Publication material for final manuscripts due: July 31, 2015.
Special section publication: March issue of 2016.

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